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EXAMINER	
QUILLEN, ALLEN E	
ART UNIT	**PAPER NUMBER**
2676	6

DATE MAILED: 01/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PR4

Office Action Summary	Application No.	Applicant(s)	
	10/010,524	WILLIS ET AL.	
	Examiner	Art Unit	
	Allen E. Quillen	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 November 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. Applicant's arguments with respect to claims 1, 9, 12, 15, 18, 23, 26 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later

invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claim 1, 3-9, 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Greene, et al, U.S. Patent 5,670,993, in view of Ohtsuka et al, U.S. Patent 6,570,802.

4. Regarding claim 1, representative of claim 9, Greene discloses a method, comprising: detecting a write command (Column 3, lines 30-34) to a frame buffer (*screen buffer,* Column 2, line 57; Column 3, lines 1-18; Column 1, lines 16-33); determining a region in the frame buffer associated with a frame buffer address in the write command (see above, Column 5, lines 48-53); and determining whether the region is the same as a last-modified region (Column 2, lines 2-20). [Claim 9, further] store the write command in memory associated with the graphics engine when the scan out logic accesses the associated region in the frame buffer (see above, Column 7, lines 59-64; *row valid, comparator,* Column 3, lines 19-29; *receives a write command WR, and a write address* ADD_{wr} *as inputs...,* Column 3, lines 31-32).

Greene discloses pixels in a row, a number or screen rows, screen memory addressing by memory row (Abstract; Column 3, lines 1-67; Column 6, lines 28-64) but does not disclose wherein the region spans more than one row of pixels. Ohtsuka teaches an entire region refresh or a partial refresh can be carried out (Column 7, lines 41-46). Power consumption reduction is the motivation for combining partial screen refresh with regions to be refreshed (Column 5, lines 30-33). Ohtsuka is evidence that at the time of the invention, it would have been obvious to one skilled in designing display memory refreshing circuits, to combine the benefits of partial screen

refresh, as Greene discloses, with regions to be refreshed, as Ohtsuka teaches, to reduce power consumption.

5. Regarding claim 3, Greene discloses the method of claim 1, further comprising: when the region is the same as the last-modified region, refraining from sending the region to the display device until a different region is detected (see above, Column 4, lines 43-50).

6. Regarding claim 4, Greene discloses the method of claim 1, wherein the write command is issued by a graphics engine to the frame buffer (see above, Column 7, lines 59-64).

7. Regarding claim 5, representative of claims 7 and 11, Greene discloses the method of claim 1, wherein the frame buffer comprises a plurality of regions each representing a plurality of pixels on a display device, and wherein the region is one of the plurality of regions (see above, *"addressable units", "redundancy units", 32-bit groups, eight bit groups,* Column 3, lines 1-18).

8. Regarding claim 6, Greene discloses the method of claim 5, wherein the plurality of regions represent the plurality of pixels in a rectangular shape on the display device (see above, *screen rows, columns, 640x480, each screen row is composed of 5,120 bit,* Figure 2, Column 2, line 58 through Column 3, line 7).

9. Regarding claim 8, Greene discloses the method of claim 4, wherein the detecting is carried out by logic connected to the frame buffer and the graphics engine (see above, *row valid,*

comparator, Column 3, lines 19-29).

Claim Rejections - 35 USC § 103

10. Claim 2, 10, 12, 15-17, 26-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Greene, et al, U.S. Patent 5,670,993, and Ohtsuka et al, U.S. Patent 6,570,802, in view of Perego, U.S. Patent 5,835,082.

11. Regarding claim 2, representative of claim 10, 12, 15-17, Greene discloses the method of claim 1, further comprising: when the sending the region to a display device associated with the frame buffer; [Claim 10, Greene further discloses] send the write command to the frame buffer (see above); [Claim 16, Greene] addresses in the writes to region numbers (*screen row information, screen row number,* Column 3, lines 30-67); [Claim 17, Greene] instructing the scan-out logic to copy the one region from the frame buffer [*screen buffer*] to the display device asynchronously from the writes to the frame buffer (*SKIP, NONSKIP, run length encoder, written to ...memory or ignored,* Column 5, line 14 through Column 6, line 27).

[Claim 12, Greene further] discloses an apparatus for writing to a display device, comprising: a frame buffer (*screen buffer,* see above) comprising a plurality of regions, wherein each region represents a respective plurality of pixels on the display device (see above); and logic to accumulate writes by a graphics engine to one of the plurality of regions in the frame

buffer until the graphics engine writes to another region of the plurality of regions in the frame buffer (see above);

Greene does not disclose wherein when the graphics engine writes to the another region, the logic is to cause the one region to be written to the display device; and, regarding Claim 2, Greene does not disclose when the region is not the same as the last-modified region, and setting the last-modified region to be the region; and, regarding Claim 10, when the scan-out logic is not accessing the associated region in the frame buffer; and regarding Claim 15, causing the one region to be written to the display device. Perego teaches wherein when the graphics engine writes to the another region, the logic is to cause the one region to be written to the display device; and when the region is not the same as the last-modified region, and setting the last-modified region to be the region; when the scan out logic is not accessing the associated region in the frame buffer; causing the one region to be written to the display device. (Column 2, lines 12-20; *As new pixel data is rendered..., full frame buffer, dirty tags for the corresponding compressed data elements are set....*, Column 2, lines 21-34). The motivation for combining frame buffered display and regions with writing to another region, setting the last-modified region to be the region displayed is to reduce bandwidth and power requirements (Column 2, lines 8-12, 42-53). Perego is evidence that at the time of the invention, it would have been obvious to one skilled in the art of frame buffer display to combine the benefits of using regions, write commands and memory addressing as Greene discloses, with regenerating unchanged frames without writing to the frame buffer and setting the last-modified region as the region displayed, as Perego teaches, to reduce bandwidth and power requirements.

Greene discloses pixels in a row, a number or screen rows, screen memory addressing by memory row (Abstract; Column 3, lines 1-67; Column 6, lines 28-64) but does not disclose wherein the region spans more than one row of pixels. Ohtsuka teaches an entire region refresh or a partial refresh can be carried out (Column 7, lines 41-46). Power consumption reduction is the motivation for combining partial screen refresh with regions to be refreshed (Column 5, lines 30-33). Ohtsuka is evidence that at the time of the invention, it would have been obvious to one skilled in designing display memory refreshing circuits, to combine the benefits of partial screen refresh, as Greene discloses, with regions to be refreshed, as Ohtsuka teaches, to reduce power consumption.

12. Regarding claim 26, representative of claims 27-30, Greene discloses an electronic device, comprising: a graphics engine to, for every respective modified region in a set of candidate regions, copy the respective modified region from a frame buffer to a display (see above).

Greene does not disclose when the respective modified region was written to during the copy, mark the respective modified region as modified, and when the respective modified region was not written to during the copy, mark the respective modified region as not modified. Petego teaches marking the modified region as not modified (*tags*, Column 2, lines 10-20). The motivation for combining regions with marking modified regions as not modified is to maintain memory coherency for subsequent frame updates, whereby unchanged frames are regenerated directly, thus saving power and bandwidth (Column 2, lines 7-20). Petego is evidence that at the time of the invention, it would have been obvious to combine the benefits of regions and writing

to display data, as Greene discloses, with marking written modified regions as unmodified, as Petego teaches, to minimize frame changes, thus saving power and bandwidth.

Claim Rejections - 35 USC § 103

13. Claims 13-14, 18-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Greene, et al, U.S. Patent 5,670,993, and Ohtsuka et al, U.S. Patent 6,570,802, in view of Perego, U.S. Patent 5,835,082, with respect to claim 12, in further view of Tsutsumi, U.S. Patent 5,333,016.

14. Regarding claim 13, representative of claims 14, 18, 19-22, Greene and Perego disclose the apparatus of claim 12, wherein the logic comprises a comparator and bit check (see above); a region number of a region currently being written to a frame buffer; wherein connected to scan-out logic, connected to a display device..

Regarding claim 13, Greene does not disclose a plurality of D-type flip-flops;

[Claim 14, further does not disclose] wherein one of the plurality of D-type flip flops is to receive input of a region number of the one region and a clock input to be active when each of the respective writes occurs;

[Claim 18-22, further does not disclose], a first data input, a first clock input to be active when a write has occurred; [Claim 19] a second D-type flip flop, a second data input coupled to a first output of the first D-type flip flop, and a second clock input coupled to compare logic output; [Claim 20] a third D-type flip flop, a third data input coupled to a second output of the second D-type flip flop, and a third clock input to be active when the write to the frame buffer

has occurred; [Claim 21] compare logic, a first compare data input coupled to the second output of the second D-type flip flop, and a second compare data input coupled to the first output of the D-type flip flop; [Claim 22] the third D-type flip flop, a third output [for displaying data].

Tsutsumi teaches a plurality of D-type flip flops (Figure 2(c), Column 4, line 39 through Column 5, line 22; Column 6, lines 54 through Column 7, line 9). The motivation for combining logic with multiple D [Data] type flip flops and a clock input associated with the write, is to provide a stable display position of the digital image, to reduce it moving up and down by one scan line (Column 4, lines 3-14; Column 7, lines 3-9), as follows: (1) the first two flip flops for a two-stage synchronizing counter with the horizontal synchronizing signal as a trigger and synchronously count two of the horizontal synchronizing signals, thereby allowing the first flip flop to latch the vertical synchronizing signal and the second flip flop causes a time delay of a single scanning interval, so that the signal for generating the trailing edge of the vertical synchronizing signal can be generated at the follow-on synchronizing signal, and (2) the third flip flop is provided between the first and second to create a synchronizing three-stage counter (Column 4, line 58 through Column 5, line 15). Apostol is evidence that at the time of the invention, it would have been obvious to one skilled in the art of the use of display memory using logic and logical methods, to combine the benefits of logical operations, as Greene discloses, with logical D-type flip flops and a clock associated with write, as Apostol teaches, to minimize bus contentions by getting set up in one clock cycle.

Greene does not disclose wherein when the graphics engine writes to the another region, the logic is to cause the one region to be written to the display device; and, regarding Claim 2, Greene does not disclose when the region is not the same as the last-modified region, and setting

the last-modified region to be the region; and, regarding Claim 10, when the scan-out logic is not accessing the associated region in the frame buffer; and regarding Claim 15, causing the one region to be written to the display device. Perego teaches wherein when the graphics engine writes to the another region, the logic is to cause the one region to be written to the display device; and when the region is not the same as the last-modified region, and setting the last-modified region to be the region; when the scan out logic is not accessing the associated region in the frame buffer; causing the one region to be written to the display device. (Column 2, lines 12-20; *As new pixel data is rendered..., full frame buffer, dirty tags for the corresponding compressed data elements are set....*, Column 2, lines 21-34). The motivation for combining frame buffered display and regions with writing to another region, setting the last-modified region to be the region displayed is to reduce bandwidth and power requirements (Column 2, lines 8-12, 42-53). Perego is evidence that at the time of the invention, it would have been obvious to one skilled in the art of frame buffer display to combine the benefits of using regions, write commands and memory addressing as Greene discloses, with regenerating unchanged frames without writing to the frame buffer and setting the last-modified region as the region displayed, as Perego teaches, to reduce bandwidth and power requirements.

Greene discloses pixels in a row, a number or screen rows, screen memory addressing by memory row (Abstract; Column 3, lines 1-67; Column 6, lines 28-64) but does not disclose wherein the region spans more than one row of pixels. Ohtsuka teaches an entire region refresh or a partial refresh can be carried out (Column 7, lines 41-46). Power consumption reduction is the motivation for combining partial screen refresh with regions to be refreshed (Column 5, lines 30-33). Ohtsuka is evidence that at the time of the invention, it would have been obvious to one

skilled in designing display memory refreshing circuits, to combine the benefits of partial screen refresh, as Greene discloses, with regions to be refreshed, as Ohtsuka teaches, to reduce power consumption.

Claim Rejections - 35 USC § 103

15. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Greene, et al, U.S. Patent 5,670,993, and Ohtsuka et al, U.S. Patent 6,570,802, in view of Perego, U.S. Patent 5,835,082, and Thacker, et al, U.S. Patent 5,276,851.

16. Regarding claim 23, Greene discloses an electronic device comprising: a frame buffer comprising a plurality of regions each representing a respective plurality of pixels on a display device; a graphics engine to initiate writes to one of the plurality of regions in the frame buffer; logic to cause the frame buffer to accumulate the writes; and scan-out logic to write the one of the plurality of regions from the frame buffer to the display device when instructed (see above).

Greene does not disclose snoop, or when instructed by the snoop logic. Thacker teaches snoop, or when instructed by the snoop logic (Column 3, lines 41-49). The motivation for combining logic with snooping is to maintain "cache [memory] coherence" address sharing with more than one processor (Column 3, lines 41-49). Thacker is evidence that at the time of the invention, it would have been obvious to one skilled in the art of frame buffer memory write commands to combine the benefits of logic and regions, as Greene discloses, with snooping, as Thacker teaches, in order to maintain a coherent memory addressing with more than one processor (Column 3, lines 44-45).

Greene does not disclose wherein when the graphics engine writes to the another region, the logic is to cause the one region to be written to the display device; and, regarding Claim 2, Greene does not disclose when the region is not the same as the last-modified region, and setting the last-modified region to be the region; and, regarding Claim 10, when the scan-out logic is not accessing the associated region in the frame buffer; and regarding Claim 15, causing the one region to be written to the display device. Perego teaches wherein when the graphics engine writes to the another region, the logic is to cause the one region to be written to the display device; and when the region is not the same as the last-modified region, and setting the last-

modified region to be the region; when the scan out logic is not accessing the associated region in the frame buffer; causing the one region to be written to the display device. (Column 2, lines 12-20; *As new pixel data is rendered..., full frame buffer, dirty tags for the corresponding compressed data elements are set....*, Column 2, lines 21-34). The motivation for combining frame buffered display and regions with writing to another region, setting the last-modified region to be the region displayed is to reduce bandwidth and power requirements (Column 2, lines 8-12, 42-53). Perego is evidence that at the time of the invention, it would have been obvious to one skilled in the art of frame buffer display to combine the benefits of using regions, write commands and memory addressing as Greene discloses, with regenerating unchanged frames without writing to the frame buffer and setting the last-modified region as the region displayed, as Perego teaches, to reduce bandwidth and power requirements.

Greene discloses pixels in a row, a number or screen rows, screen memory addressing by memory row (Abstract; Column 3, lines 1-67; Column 6, lines 28-64) but does not disclose wherein the region spans more than one row of pixels. Ohtsuka teaches an entire region refresh or a partial refresh can be carried out (Column 7, lines 41-46). Power consumption reduction is the motivation for combining partial screen refresh with regions to be refreshed (Column 5, lines 30-33). Ohtsuka is evidence that at the time of the invention, it would have been obvious to one skilled in designing display memory refreshing circuits, to combine the benefits of partial screen refresh, as Greene discloses, with regions to be refreshed, as Ohtsuka teaches, to reduce power consumption.

Claim Rejections - 35 USC § 103

17. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Greene, et al, U.S. Patent 5,670,993, in view of Perego, U.S. Patent 5,835,082, and Thacker, et al, U.S. Patent 5,276,851, as applied to claim 23, in further view of Tsutsumi, U.S. Patent 5,333,016.

18. Regarding claim 24, Greene discloses the electronic device of claim 23, wherein there is display and memory logic (see above).

Greene does not disclose snoop logic comprises a plurality of D-type flip-flops.

Greene does not disclose snoop, or when instructed by the snoop logic. Thacker teaches snoop, or when instructed by the snoop logic (Column 3, lines 41-49). The motivation for combining logic with snooping is to maintain "cache [memory] coherence" address sharing with more than one processor (Column 3, lines 41-49). Thacker is evidence that at the time of the invention, it would have been obvious to one skilled in the art of frame buffer memory write commands to combine the benefits of logic and regions, as Greene discloses, with snooping, as Thacker teaches, in order to maintain a coherent memory addressing with more than one processor (Column 3, lines 44-45).

Tsutsumi teaches a plurality of D-type flip flops (Figure 2(c), Column 4, line 39 through Column 5, line 22; Column 6, lines 54 through Column 7, line 9). The motivation for combining logic with multiple D [Data] type flip flops and a clock input associated with the write, is to provide a stable display position of the digital image, to reduce it moving up and down by one scan line (Column 4, lines 3-14; Column 7, lines 3-9), as follows: (1) the first two flip flops for a

two-stage synchronizing counter with the horizontal synchronizing signal as a trigger and synchronously count two of the horizontal synchronizing signals, thereby allowing the first flip flop to latch the vertical synchronizing signal and the second flip flop causes a time delay of a single scanning interval, so that the signal for generating the trailing edge of the vertical synchronizing signal can be generated at the follow-on synchronizing signal, and (2) the third flip flop is provided between the first and second to create a synchronizing three-stage counter (Column 4, line 58 through Column 5, line 15). Apostol is evidence that at the time of the invention, it would have been obvious to one skilled in the art of the use of display memory using logic and logical methods, to combine the benefits of logical operations, as Greene discloses, with logical D-type flip flops and a clock associated with write, as Apostol teaches, to minimize bus contentions by getting set up in one clock cycle.

Claim Rejections - 35 USC § 103

19. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Greene, et al, U.S. Patent 5,670,993, in view of Perego, U.S. Patent 5,835,082, Thacker, et al, U.S. Patent 5,276,851, and Tsutsumi, U.S. Patent 5,333,016, with respect to claims 23 and 24, in further view of Bell, U.S. Patent 4,958,378.

20. Regarding claim 25, Greene, Perego, Thacker and Tsutsumi disclose the electronic device of claim 24 (see above). Greene does not disclose wherein the D-type flip-flop further comprises an exclusive-OR gate.

Tsutsumi teaches a plurality of D-type flip flops (Figure 2(c), Column 4, line 39 through Column 5, line 22; Column 6, lines 54 through Column 7, line 9). The motivation for combining logic with multiple D [Data] type flip flops and a clock input associated with the write, is to provide a stable display position of the digital image, to reduce it moving up and down by one scan line (Column 4, lines 3-14; Column 7, lines 3-9), as follows: (1) the first two flip flops for a two-stage synchronizing counter with the horizontal synchronizing signal as a trigger and synchronously count two of the horizontal synchronizing signals, thereby allowing the first flip flop to latch the vertical synchronizing signal and the second flip flop causes a time delay of a single scanning interval, so that the signal for generating the trailing edge of the vertical synchronizing signal can be generated at the follow-on synchronizing signal, and (2) the third flip flop is provided between the first and second to create a synchronizing three-stage counter (Column 4, line 58 through Column 5, line 15). Apostol is evidence that at the time of the invention, it would have been obvious to one skilled in the art of the use of display memory using logic and logical methods, to combine the benefits of logical operations, as Greene discloses, with logical D-type flip flops and a clock associated with write, as Apostol teaches, to minimize bus contentions by getting set up in one clock cycle.

Greene does not disclose an exclusive-OR gate. Bell teaches an exclusive-OR gate (Column 7, lines 1-34). The motivation for combining logic with logic using an exclusive OR

gate is, during writing into memory, the current data and the incoming data can be compared to determine if the new data has changed in a memory cycle (Column 7, lines 4-11). Bell is evidence that at the time of the invention, it would have been obvious to combine the benefits of logic during writing to memory, as Greene disclose, with an exclusive-OR gate, as Bell teaches, to determine in the new data had changed.

Prior Art Not Used

The Examiner provides the following relevant art:

Song, U.S. Patent 6,094,705, explicitly teaches selective refresh for a memory array in multiple memory rows in, for example, notebook computers where eliminating unnecessary power consumption is critically important in prolonging the battery life.

Response to Arguments

21. Applicant's arguments and amendments with respect to claims 1, 9, 12, 15, 18, 23, 26 have been considered but are moot in view of the new ground(s) of rejection. Additional search and consideration were required.

22. The Applicant asserts that selective or sparse [partial] refresh of a pixel region is part of the inventive concept, whereas reference Greene [Display Refresh System Having Reduced Memory Bandwidth, U.S. Patent 5,670,993] teaches individual pixel rows (Page 7, 5th Paragraph; Pages 9, 1st Paragraph; 10, 2nd, 7th Paragraphs), thus the amendments to particularly claim and point out this distinctive feature. Furthermore, Greene does not teach "determining whether the region is the same as a last modified. (Page 8, 2nd Paragraph)."

The Examiner respectfully notes this amendment in the amended independent claims, thus a new reference, Ohtsuka [and Song], are provided.

The point that Greene does not teach "determining whether the region is the same as a last modified" is without merit. Greene's words are, *"redundancy memory, repeat bit, the value of the repeat bit indicates whether or not the addressable unit is identical to the previous addressable unit. The repeat bit takes one of two states: SKIP (meaning identical to the previous addressable unit)...."* (Column 2, lines 2-20).

23. The Applicant asserts that Greene and Perego cannot be combine and there is no motivation within the art to combine them (Page 10, 1st Paragraph).

The Examiner respectfully replies, however, that Perego in Video **Refresh** Compression, documents a high performance, high resolution, high color graphics display without increased power consumption, and with reduced bandwidth, that auto-regenerates unchanged frame buffer pixel data at high refresh rates (Column 1, lines 21-34, 60-67; Column 2, lines 6-20). This feature, Perego states, enables unified memory using DRAM (Column 2, lines 48-52). Perego is evidence that a better way was needed to reduce power consumption and increase bandwidth in a graphics display design domain (Column 3, lines 24-27), and that part of the answer is avoiding refreshing data elements in **the entire image** in the frame buffer, and that the display is updated, in one case noted by Perego, 92 % of the time without the high costs of refresh in the conventional sense.

Conclusion

24. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Allen E. Quillen whose telephone number is (703) 605-4584. The examiner can normally be reached on Tuesday – Friday, 8:30am – noon and 1:00 - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew C. Bella, can be reached on (703) 308-6829.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Or FAX'd to:

(703) 872-9314 (for Technology Center 2600 only)

Hand delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Sixth Floor (Receptionist), Arlington, Virginia

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number (703) 305-9600 or (703) 305-3800.

Allen E. Quillen
Patent Examiner
Art Unit 2676

***January 12, 2004

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